Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.087”**

**.082”**

**SOURCE**

**GATE**

**Top Material: Al**

**Backside Material: CrNiAg**

**Bond Pad Size: S = .017” X .027” G = .016” X .025”**

**Backside Potential: DRAIN**

**Mask Ref: HEX 1**

**APPROVED BY: DK DIE SIZE .082” X .087” DATE: 11/9/21**

**MFG: INT’L RECTIFIER THICKNESS .019” P/N: IRFC9210**

**DG 10.1.2**

#### Rev B, 7/19/02